(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) EP 0 858 103 A2

(12) EUROPEAN PATENT APPLICATION

(43) Date of publication:
12.08.1998 Bulletin 1998/33

(51) Int Cl.⁶: H01L 21/3213, H01L 21/285

(21) Application number: 98300564.6

(22) Date of filing: 27.01.1998

(84) Designated Contracting States:
AT BE CH DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE
Designated Extension States:
AL LT LV MK RO SI

(30) Priority: 05.02.1997 KR 9703580
09.06.1997 KR 9723660

(71) Applicant: Samsung Electronics Co., Ltd.
Suwon City, Kyungki-do (KR)

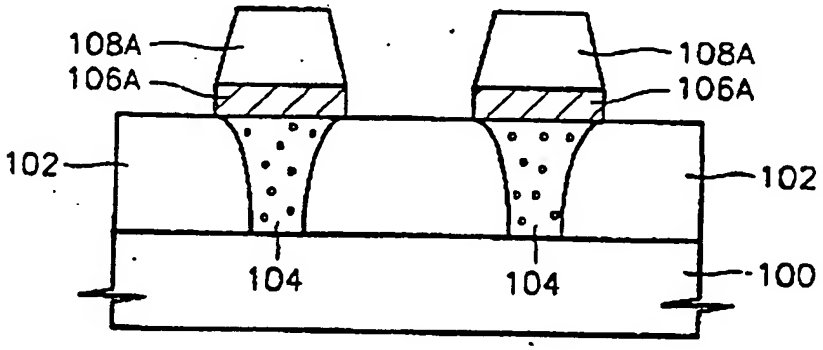
(72) Inventors:
- Kim, Hyoun-woo
Seocho-gu, Seoul (KR)
- Nam, Byeong-yun
Paldal-gu, Suwon-city, Kyungki-do (KR)
- Ju, Byong-sun
Songpa-gu, Seoul (KR)
- Yoo, Won-jong
Songpa-gu, Seoul (KR)

(74) Representative: Clugg, David John et al
Appleyard Lees,
15 Clare Road
Halifax, West Yorkshire HX1 2HY (GB)

(54) Method for etching Pt film of semiconductor device

(57) A method for improving the etching slope in etching a Pt layer used as a storage node of a semiconductor device is provided. By the method, an adhesive layer (110) including Ti on the Pt layer (108) is changed to TiOx, by using an etching gas containing oxygen, to act as an additional etching mask. The Pt layer (108) is overetched by using the fact that the TiOx layer is formed to avoid overall erosion of the adhesive layer mask at a predetermined temperature, i.e., 120 ~ 300°C, to thereby improve the etching slope of the Pt layer.

FIG. 5



EP 0 858 103 A2

Description

The present invention relates to a fabrication method of a semiconductor memory device, and more particularly, to a method for etching a Pt film which is used as a storage node of a capacitor of a semiconductor memory device.

In general, as the degree of integration of the semiconductor memory device becomes higher, a semiconductor memory device such as a dynamic random access memory (DRAM) requires a capacitor of high capacitance and at the same time occupying a small area. Accordingly, a trench type or cylinder type capacitor has been developed. However, the trench type or cylinder type capacitor is fabricated by a complicated process, and it is difficult to form correctly. Thus, there is a limit to realizing high capacitance and high integration, which are required for the integrated semiconductor memory device.

With a view to solving this problem, there has been provided a method for forming a capacitor, using barium strontium titanate (BST) as a dielectric of the capacitor. BST has a dielectric constant higher than that of a conventional dielectric. In the case that the capacitor is formed using a material of high dielectric constant such as BST, a Pt layer is usually used as plate and storage nodes of the capacitor. This is because the Pt is stable material which does not oxidize at the surface of a dielectric during high-temperature heat treatment for forming of a BST dielectric film. Moreover, Pt has excellent conductivity and less leakage current generated from the dielectric electrode of the capacitor than other conductive films such as Ir, Ru, or polysilicon. However, Pt is very difficult to pattern using dry etching. This is because Pt is an unreactive metal and thus it does not react with other chemicals easily. Halogen is usually used for the reactive ion etching (RIE) for etching the Pt layer, but halogen reacts weakly with Pt ions, so the Pt layer is etched not by chemical reaction, but by physical reaction of sputtering. Accordingly, in the case that the Pt layer is etched by ion sputtering, etching residues are generated, which reduce the etching slope of the Pt layer. Therefore, Pt electrodes do not have fine pattern. Also, in order to improve the low etch rate during reactive ion etching, an etching gas containing chlorine or fluorine is used.

A conventional method for etching the Pt layer, using chlorine gas as an etching gas, is disclosed in U.S. Patent No. 5,515,984 'Method for etching Pt layer', issue date May, 14, 1996. Here, chlorine and oxygen is used as an etching gas, and thus etching residues PtCl and PtO are formed on the sidewalls of an etching resist film so that the Pt layer is etched by using the etching resist film and the etching residues as an etching mask. After that the etching residues are removed by wet etching.

However, the etching residues require appropriate removal, and also the etching slope of the Pt layer is still to be improved.

With a view to solve or reduce the above problems, it is an aim of preferred embodiments of the present invention to provide a method for etching a Pt layer of a semiconductor device, in which a semiconductor substrate where a Pt layer is formed is heated to a predetermined temperature to overetch the Pt layer, using an adhesive layer containing titanium as an etching mask on the Pt layer, to thereby improve an etching slope of the sidewall of the Pt layer.

According to an aspect of the invention, there is provided a method for etching a Pt layer of a semiconductor device wherein, a barrier layer, a Pt layer, an adhesive layer containing Ti and a mask layer are sequentially formed on the semiconductor substrate where a bottom layer is formed. Then, the mask layer is patterned to form a mask pattern, and the adhesive layer is patterned using the mask pattern. At this time, the patterning is preferably performed by dry etching, using Ar/Cl as an etching gas. The resultant structure is preferably heated to 120 ~ 300°C without exciting a plasma. Subsequently, the Pt layer may be etched, using a patterned mask layer and a patterned adhesive layer formed on the semiconductor substrate, and the mask pattern on the Pt layer removed by overetching.

According to a further aspect, there is provided a method for etching a Pt layer of a semiconductor device, comprising steps of: forming the Pt layer on the semiconductor substrate where a bottom layer is formed; forming an adhesive layer on the Pt layer; forming a mask layer on the adhesive layer; patterning the mask layer to form a mask pattern; patterning the adhesive layer using the mask pattern; heating the semiconductor substrate in a plasma etching apparatus; etching the Pt layer using the mask pattern and the patterned adhesive layer; and removing the mask pattern.

A barrier layer is preferably formed on the bottom layer before the step of forming the Pt layer.

Preferably, the mask layer is composed of one or more layers including an oxide layer. Also, it is preferable that the adhesive layer contains Ti and the barrier layer is formed of TiN or a material containing TiN. The bottom layer includes preferably a first insulating layer having contact holes formed on the semiconductor substrate. Here, each contact hole is preferably buried with a polysilicon plug. The Pt layer is preferably etched by an etching gas containing O_2. The etching gas may be O_2/Cl_2, O_2/HBr, O_2/Br_2 or O_2/Br. The etching gas is preferably at least 50% oxygen.

Preferably, the Pt layer is patterned by magnetically enhanced reactive ion etching (MERIE) method, using O_2/Cl_2 as an etching gas, where the oxygen is 50% or more of the total O_2/Cl_2 mixture.

Preferably, the Mask pattern is removed by overetching past the end of etching the Pt layer.

Also, the overetching for removing the mask pattern is preferably performed by extending the etching time by 0.5 - 1.5 times as much as the etching time required to etch up to etching end point of Pt layer, and the ad-

hesive layer and the barrier layer are patterned using Ar/Cl_2 as the etching gas.

According to embodiments of the present invention, the semiconductor substrate where the Pt layer is formed is heated to a predetermined temperature to overetch the Pt layer, using an adhesive layer containing titanium as an etching mask on the Pt layer, to thereby improve the etching slope of the sidewall of the Pt layer.

For a better understanding of the invention, and to show how embodiments of the same may be carried into effect, reference will now be made, by way of example, to the accompanying diagrammatic drawings, in which:

Figures 1 through 5 are sectional views illustrating a method for etching a Pt layer of a semiconductor device according to a preferred embodiment of the present invention.

A mask layer indicated in the present invention does not necessarily mean one layer. For example, the mask layer formed of an oxide layer may be formed of a plurality of layers, including an oxide layer.

Referring to Figure 1, a bottom layer is formed on a semiconductor substrate 100 where a lower structure such as a transistor(not shown) is formed. The bottom layer is a layer obtained by stacking a first insulating layer, for example, an interlayer dielectric 102, on the semiconductor substrate 100, and further performing patterning to form a contact hole, and then burying the contact hole with a polysilicon plug 104. Subsequently, the semiconductor substrate is planarized by performing a planarization process such as etchback or chemical mechanical polishing the resultant structure of the bottom layer. A barrier layer 106, for preventing deterioration of capacitor performance due to interdiffusion of the polysilicon plug 104 and the Pt layer 108, is formed on the entire surface of the resultant structure where the planarization has been performed. Here, the barrier layer 106 is formed to a thickness of 300 ~ 700Å, using TiN or a material containing TiN. Subsequently, Pt is deposited on the barrier layer 106 in a usual manner such as sputtering or chemical vapor deposition (CVD), to form the Pt layer 108. In an embodiment of the present invention, the Pt layer 108, being a conductive layer used as a storage node of a capacitor in a semiconductor memory device, is formed to a thickness of 2900Å ± 500Å.

Referring to Figure 2, an adhesive layer for enhancing adhesion of a mask layer to the Pt layer 108 is formed on the resultant structure where the Pt layer 108 is formed, using Ti. The adhesive layer in the present embodiment is 400 ~ 800Å thick. Subsequently, the mask layer of 5000Å ± 1000Å is formed on the adhesive layer, using an oxide layer. The mask layer is coated with photoresist, and a usual photolithographic process is performed to form a mask pattern 112. The mask layer, which is formed as one oxide layer in the embodiment, may be a composite layer containing the oxide layer. Then, the adhesive layer is patterned using the mask pattern 112 as an etching mask, to form an adhesive layer mask pattern 110 contacting the mask pattern 112. At this time, the adhesive layer is patterned by dry etching, for example, magnetically enhanced RIE (MERIE), using Ar/Cl_2 as an etching gas.

Referring to Figure 3, the resultant structure where the mask pattern 112 and the adhesive layer mask pattern 110 are formed is heated to 120 ~ 300°C, with an exciting a plasma of the MERIE equipment. Subsequently, the Pt layer 108 is etched until the barrier layer 106 of a lower portion is exposed, using a mixture containing O_2 i.e., Cl_2/O_2, HBr, Br_2 or Br as an etching gas, and the mask pattern 112 and the adhesive layer mask pattern 110 as an etching mask. At this time, it is preferable that O_2 of the mixture is at least 50%. In the present embodiment, oxygen and chlorine are mixed at 4:1. Accordingly, ions and radicals of the O_2 gas are species for sputtering the Pt layer. Also, the O_2 gas increases an etching selection ratio of the Pt layer 108 with respect to the mask pattern 112 formed of an oxide layer, and changes the Ti layer of the adhesive layer mask pattern 110 into TiOx. TiOx acts as an additional etching mask pattern during etching the Pt layer. That is, a portion of O_2 ions and radicals partially oxidize the Ti layer into the TiOx layer, to reduce erosion velocity of the mask.

Figure 4A is a sectional view of a Pt layer 108A having an enhanced etching slope through overetching the Pt layer 108 under the same etching conditions as those of Figure 3. At this time, the mask pattern 112 erodes away completely and thus is removed during the overetching. At this time, it is preferable that the overetching is performed by extending the etching time by 0.5 ~ 1.5times as much as the etching time_required to expose the barrier layer 106, i.e., an etching end point as shown in Figure 3. When the etching gas of $O_2/Cl_2/Ar$ is used, the etching slope of the Pt layer 108, having a pitch of 0.59μm and a thickness of 2000Å, is 65° or less. This is because the Pt does not react with oxygen and chlorine. However, when the Pt layer 108A is etched using an etching gas containing much oxygen, Ti forming the adhesive layer mask pattern 110 formed on the Pt layer is converted to TiOx, to act as an additional mask pattern together with an oxide layer mask pattern being the mask pattern 112. At this time, the adhesive layer mask pattern 110 of TiOx is eroded at a high temperature of 120 ~ 300°C by a degree equivalent to that at a room temperature. Accordingly, high temperature hastens oxidation of Ti, and thus erosion by oxygen ions or sputtering of a radical is relatively reduced, so that the mask pattern is not damaged at a high temperature. The adhesive layer mask pattern having little erosion acts as a factor for improving the etching slope of the Pt layer 108A. That is, when overetching is performed at below 120°C, the adhesive layer mask pattern 110A containing Ti begins to be rapidly eroded from an edge by sputtering. However, when the overetching is performed at a temperature of 150°C or more, the adhesive layer mask pattern 110A is not eroded, even after the mask

pattern 112 is removed, and thus the etching slope of the sidewall of the Pt layer 108A is close to vertical. At this time, Ti of the adhesive layer pattern 110A is converted to TiOx more rapidly than that of the adhesive layer pattern etched at below 120°C. When the temperature of the MERIE chamber is set at 160°C and the surface temperatur of the semiconductor substrate is set at 140°C, the etching slope θ1 of the Pt layer 108A is improved to be approximately 80°. The temperature of 120 ~ 300°C indicates the temperature of a semiconductor substrate surface. According to embodiments of the present invention, the over etching of the Pt layer 108A and the controlled etching temperature may improve the etching slope of the Pt layer.

Figure 4B is a sectional view of a semiconductor substrate after etching at 120°C or less to compare to the result of Figure 4A. At this time, the mask pattern 112 is eroded and removed, and then the edges of the adhesive layer mask pattern 110B are also eroded, which causes the sidewall slope thereof to be approximately 45°. Accordingly, when the Pt layer is etched through sputtering, the adhesive layer mask pattern 110B cannot improve the etching slope. For example, when the over etching is performed under the conditions where the chamber is at 130°C, and the semiconductor substrate surface is at 120°C, the etching slope θ2 of the Pt layer 108B is 72° or less.

Figure 5 is a sectional view of a semiconductor substrate after the mask pattern is overetched, and then the adhesive layer mask pattern 110A is removed from the Pt layer 108A, and further a barrier layer 106 under the Pt layer 108A is patterned. At this time, Ar/Cl_2 is used as the etching gas for removing the adhesive layer mask pattern 110A and patterning the barrier layer 106A. Therefore, the etching of the Pt layer 108A including the barrier layer 106A on a polysilicon plug 104 is completed.

Example: relationship between the etching temperature and the etching slope of a Pt layer

Pt layers were overetched at etching chamber temperatures of 100°, 130°C and 160°C, respectively, and then etching slope of the sidewall of each Pt layer was measured. At this time, the Pt layer was 2000Å thick, the adhesive layer on the Pt layer was 600Å thick, and the mask pattern formed of an oxide layer was 5000Å thick. As a result, when the temperature of the etching chamber was 100°C, 130°C and 160°C, the etching slope of the sidewall of the Pt layer was 71°, 72° and 80, respectively. In the cases that the temperature of the etching chamber was 100°C and 130°C, respectively, the etching slope was not much enhanced. However, in the case that the temperature of the etching chamber was 160°C, it was remarkably enhanced.

This was because when the over etching was performed at an etching chamber temperature of 100°C, the mask pattern formed of an oxide layer is eroded and removed, and then the edges of the adhesive layer converted to Ti or TiOx under the mask pattern are continuously eroded, so that the adhesive layer was shown 800Å thick at the center, which caused the etching slope of the sidewall of the adhesive layer to be 45°. Also, when the over etching was performed at an etching chamber temperature of 130°C, the thickness of the adhesive layer on the Pt layer was 600Å at the center, however, 400Å at the edges. Accordingly, the adhesive layer was eroded too much to enhance the etching slope.

However, when the etching chamber is set at 160°C and the surface of the semiconductor substrate is at 140°C, even though the uppermost mask pattern is eroded, the adhesive layer thereunder is not eroded. That is, the adhesive layers are 600Å thick at both the edge and the center, and have sidewalls close to vertical. Accordingly, it may be possible to prevent the reduction of the etching slope of the Pt layer due to Pt atoms through sputtering while the Pt layer is anisotropically etched.

Meanwhile, when the etching was performed under the above-described conditions, the respective etch rates at 100°C, 130°C and 160°C were 395Å/min, 368Å/min and 371Å/min. When a new volatile compound is formed on the sidewall of the Pt layer to improve the etching slope, the etch rate also increases according to the temperature. However, in the case the resultant values were similar at all temperatures. Accordingly, the etch rate of the Pt layer sidewall was not improved by the chemical reaction generated from the Pt layer.

According to embodiments of the present invention, the etching slope of the Pt layer used as plate and storage nodes of the capacitor may be improved, using the fact that the erosion degree of the adhesive layer used as an additional etching mask during the Pt layer changes according to the temperature.

It should be understood that the invention is not limited to the illustrated embodiment and that many changes and modifications can be made within the scope of the invention by a person skilled in the art.

The reader's attention is directed to all papers and documents which are filed concurrently with or previous to this specification in connection with this application and which are open to public inspection with this specification, and the contents of all such papers and documents are incorporated herein by reference.

All of the features disclosed in this specification (including any accompanying claims, abstract and drawings), and/or all of the steps of any method or process so disclosed, may be combined in any combination, except combinations where at least some of such features and/or steps are mutually exclusive.

Each feature disclosed in this specification (including any accompanying claims, abstract and drawings), may be replaced by alternative features serving the same, equivalent or similar purpose, unless expressly stated otherwise. Thus, unless expressly stated otherwise, each feature disclosed is one example only of a

generic series of equivalent or similar features.

The invention is not restricted to the details of the foregoing embodiment(s). The invention extends to any novel one, or any novel combination, of the features disclosed in this specification (including any accompanying claims, abstract and drawings), or to any novel one, or any novel combination, of the steps of any method or process so disclosed.

Claims

1. A method for etching a Pt layer of a semiconductor device, comprising steps of:

   forming the Pt layer (108) on the semiconductor substrate where a bottom layer (100-106) is formed;

   forming an adhesive layer (110) on the Pt layer (108);

   forming a mask layer (112) on the adhesive layer (110);

   patterning the mask layer (112) to form a mask pattern;

   patterning the adhesive layer (110) using the mask pattern;

   heating the semiconductor substrate in a plasma etching apparatus;

   etching the Pt layer (108) using the mask pattern and the patterned adhesive layer (110); and

   removing the mask pattern.

2. The method of claim 1, wherein a barrier layer (106) is formed on the bottom layer before the step of forming the Pt layer (108).

3. The method of claim 2, wherein the barrier layer (106) is formed using TiN or a material containing TiN.

4. The method of claim 1, 2 or 3, wherein the adhesive layer (110) is formed using Ti.

5. The method of claim 1, 2, 3 or 4, wherein the mask layer consists of one or more layers.

6. The method of claim 5, wherein the one or more layers comprise one or more oxide layers.

7. The method of any of the preceding claims, wherein the semiconductor substrate is heated while no plasma is excited.

8. The method of any of the preceding claims, wherein the semiconductor substrate is heated to be within 120 ~ 300°C.

9. The method of any of the preceding claims, wherein the Pt layer is etched by an etching gas containing O_2.

10. The method of claim 9, wherein the etching gas containing O_2 is O_2/Cl_2.

11. The method of claim 10, wherein the etching gas of O_2/Cl_2 contains at least 50% oxygen.

12. The method of claim 9, wherein the etching gas containing O_2 is one selected from the group consisting of HBr, Br2 and Br.

13. The method of claim 12, wherein the etching gas of O_2/Br contains at least 50% oxygen.

14. The method of any of the preceding claims, wherein the mask pattern is removed by overetching past the end of etching the Pt layer (108).

15. The method of claim 14, wherein the overetching is performed by extending the etching time by 0.5 ~ 1.5% times as much as the etching time required to etch up to etching end point of Pt layer (108).

16. The method of claim 2 or any of claims 3 to 15 as dependent thereon, wherein the barrier layer (106) is patterned after removing the mask pattern.

17. The method of claim 16, wherein the barrier layer (106) is patterned by dry etching using Ar/Cl_2 as the etching gas.

FIG. 1

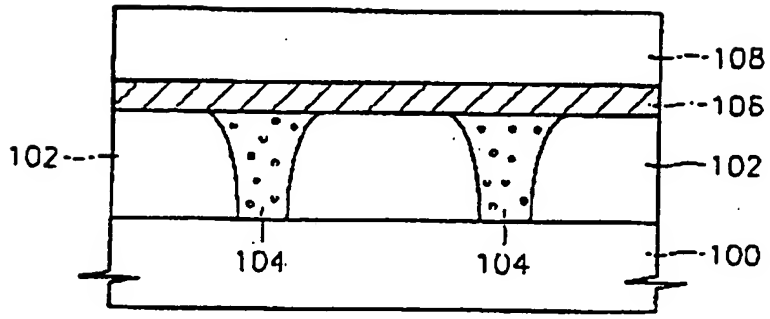


FIG. 2

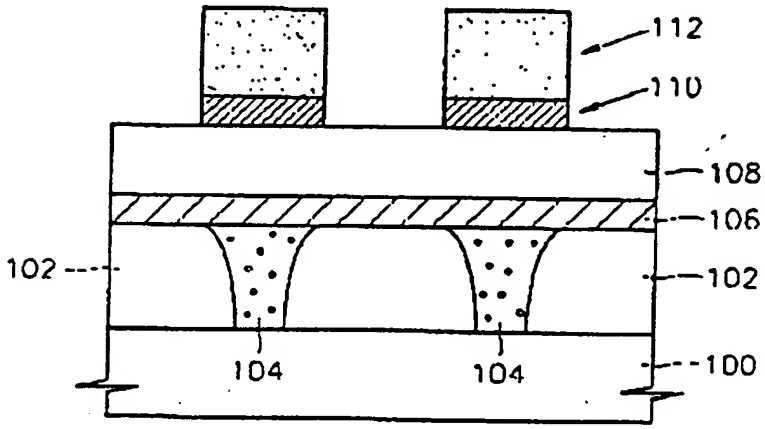


FIG. 3

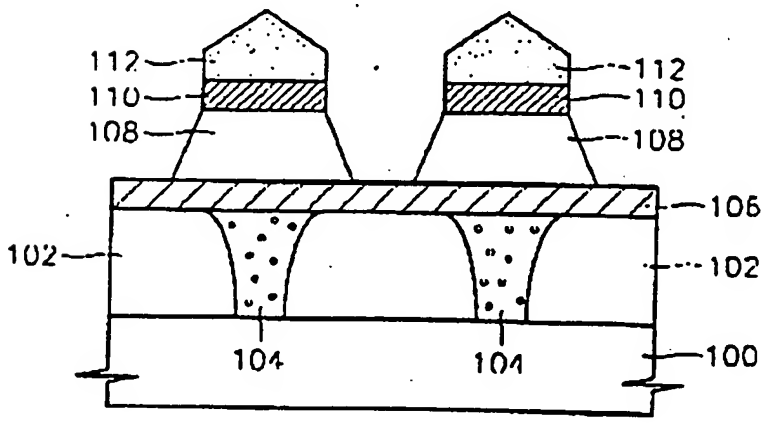


FIG. 4A

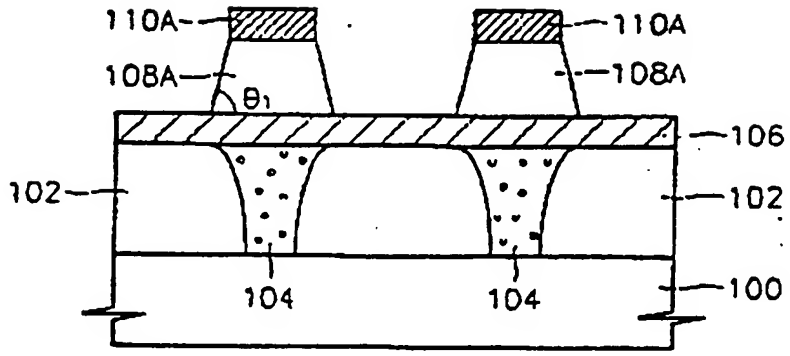


FIG. 4B

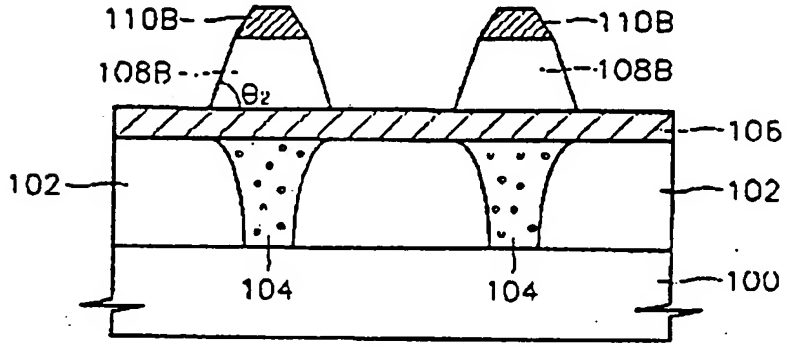


FIG. 5